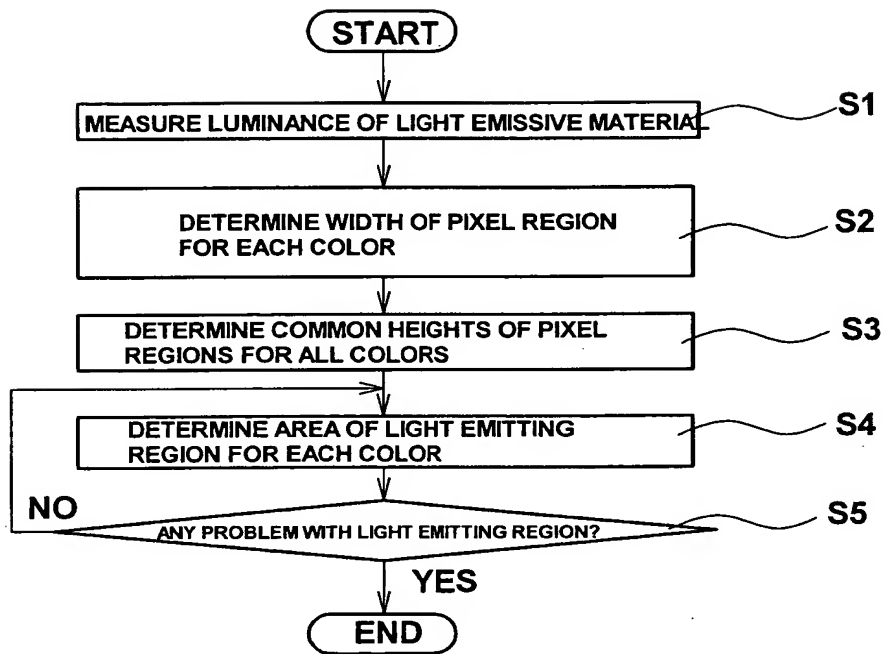
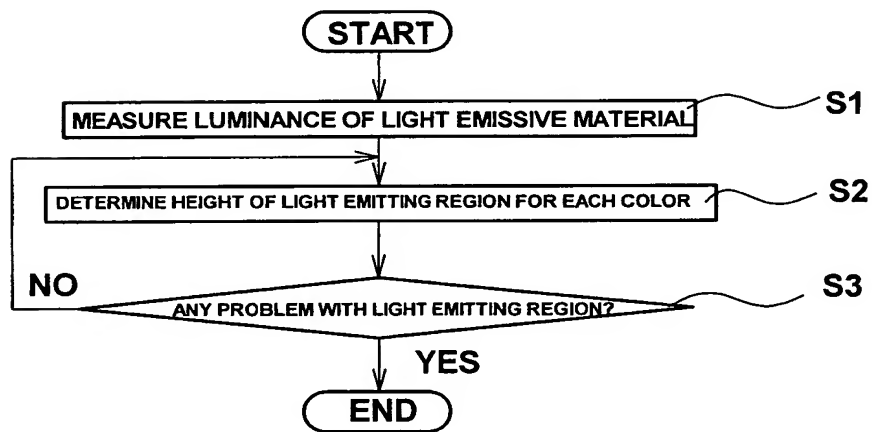


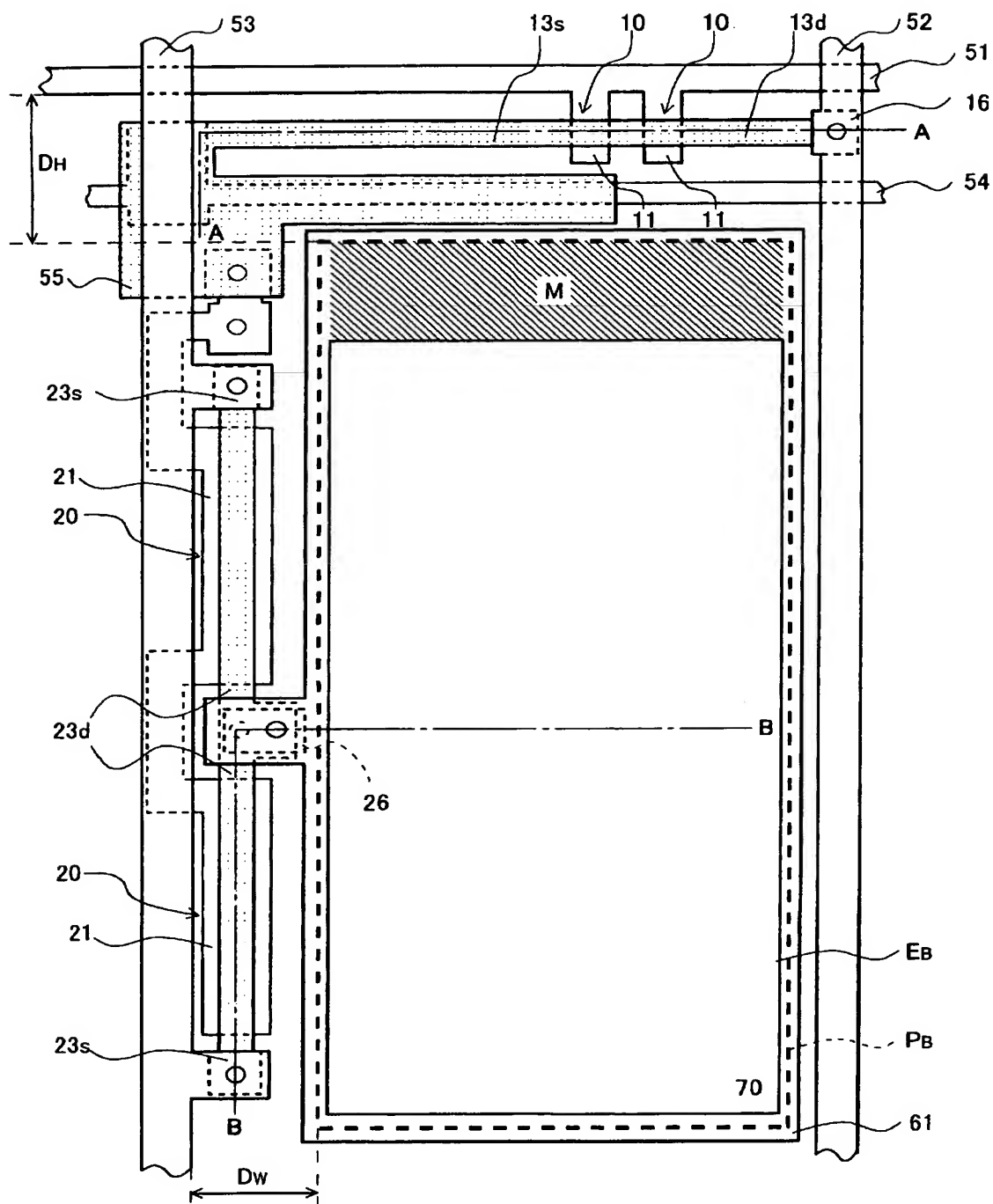
Fig. 1



**Fig. 2A**



**Fig. 2B**



**Fig. 3**

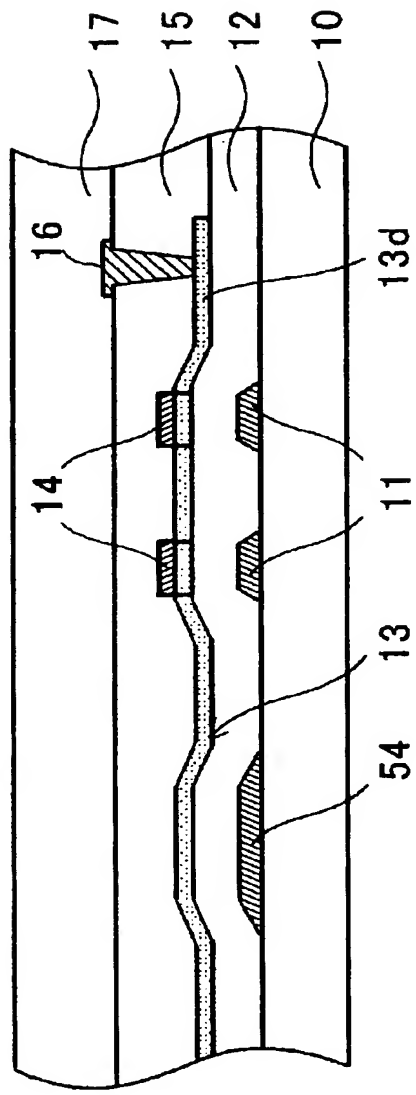
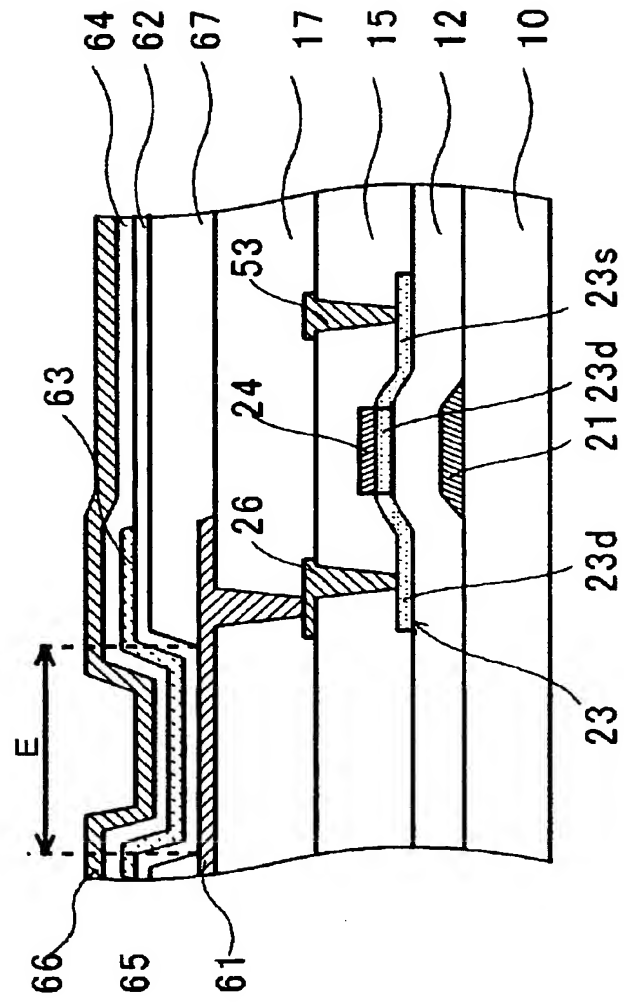


Fig. 4A



**Fiş 4B**

Fig. 5A

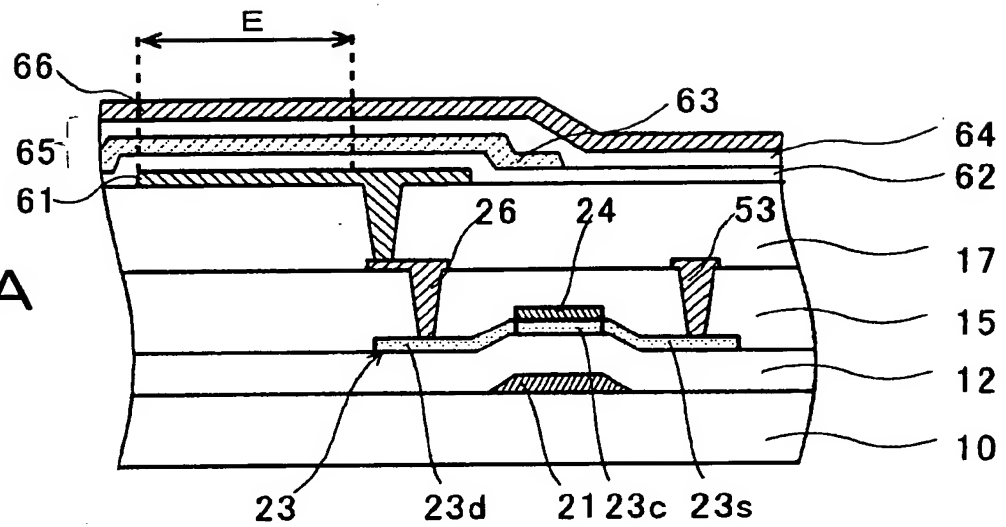


Fig. 5B

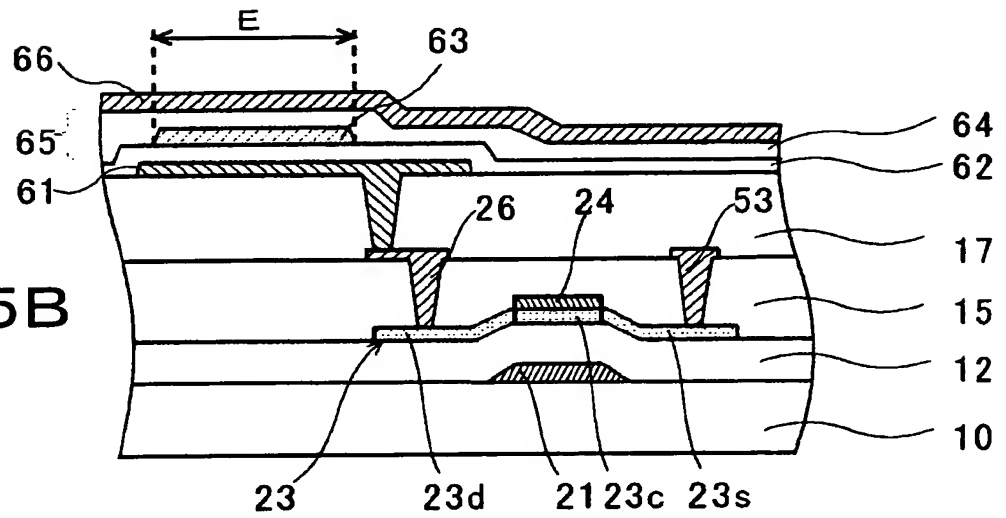


Fig. 6A

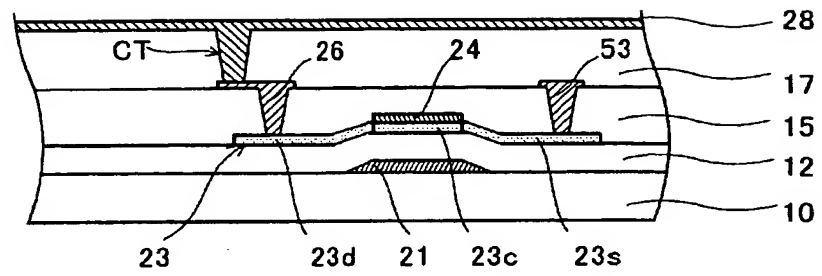


Fig. 6B

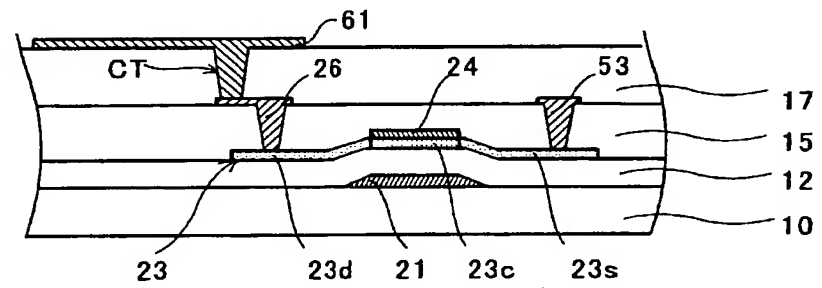


Fig. 6C

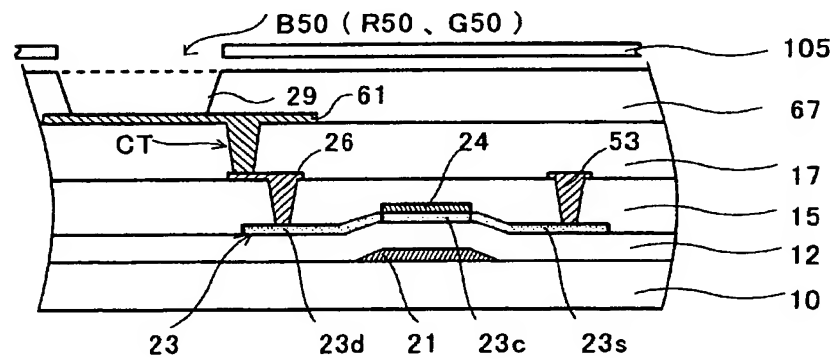
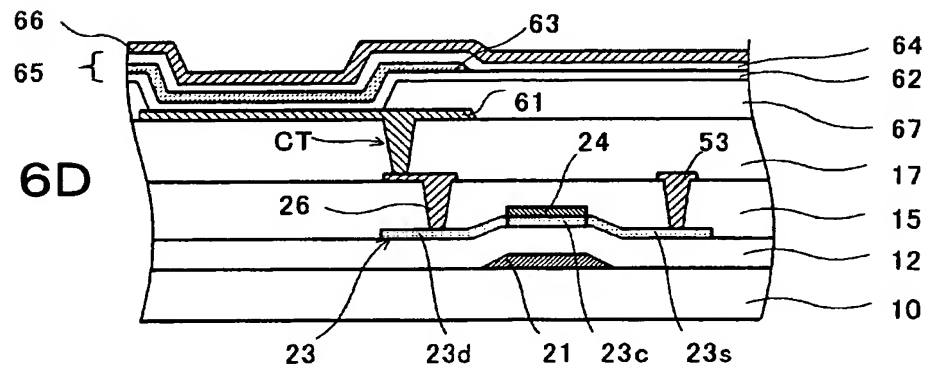


Fig. 6D



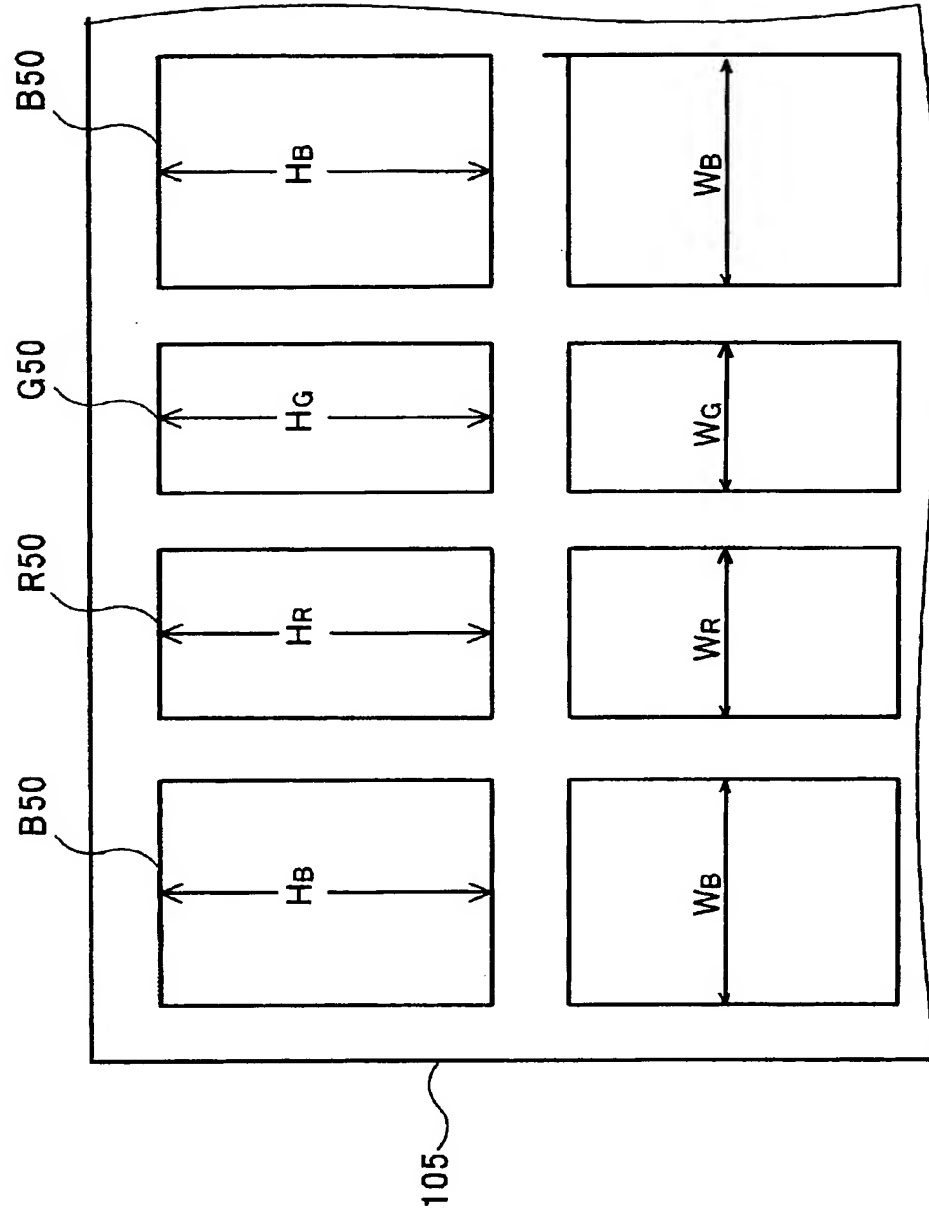


Fig. 7

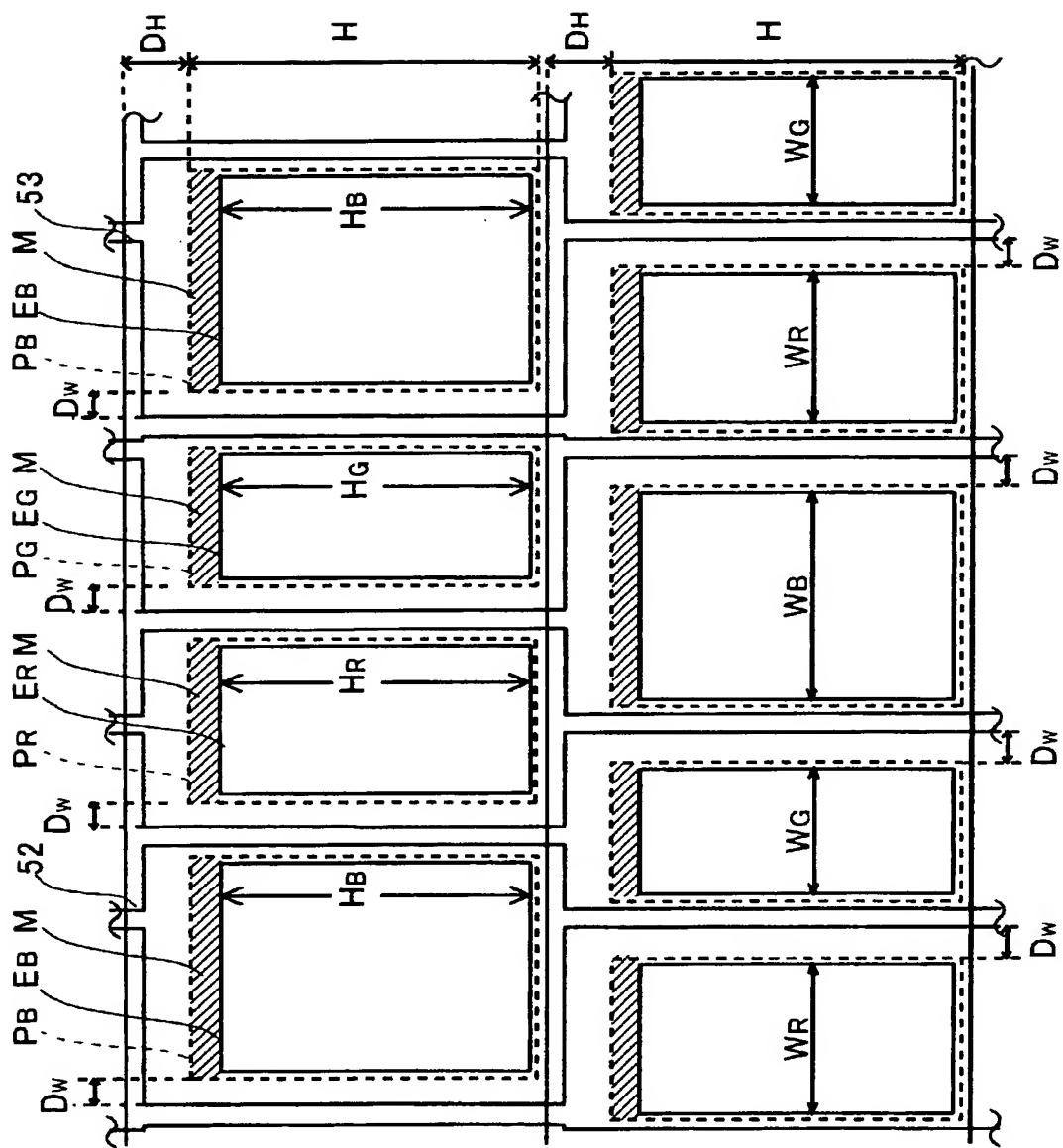


Fig. 8



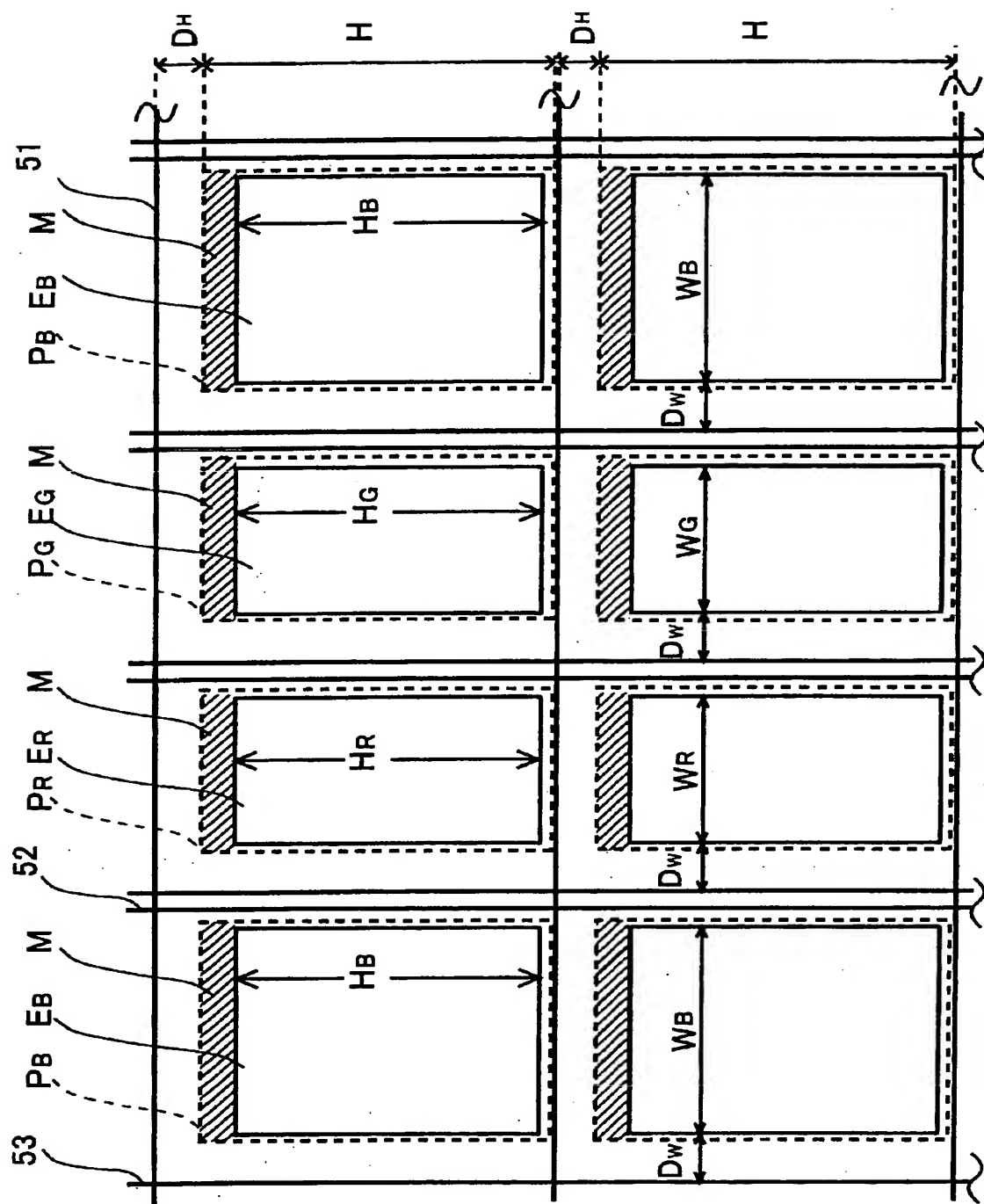


Fig. 9



**Fig. 10**

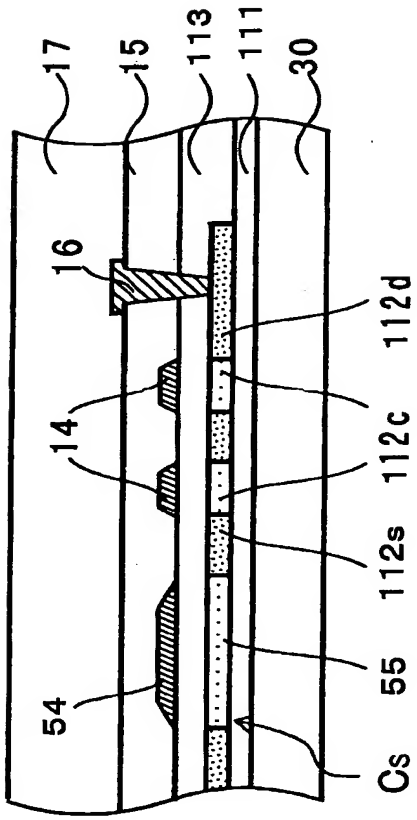


Fig. 11A

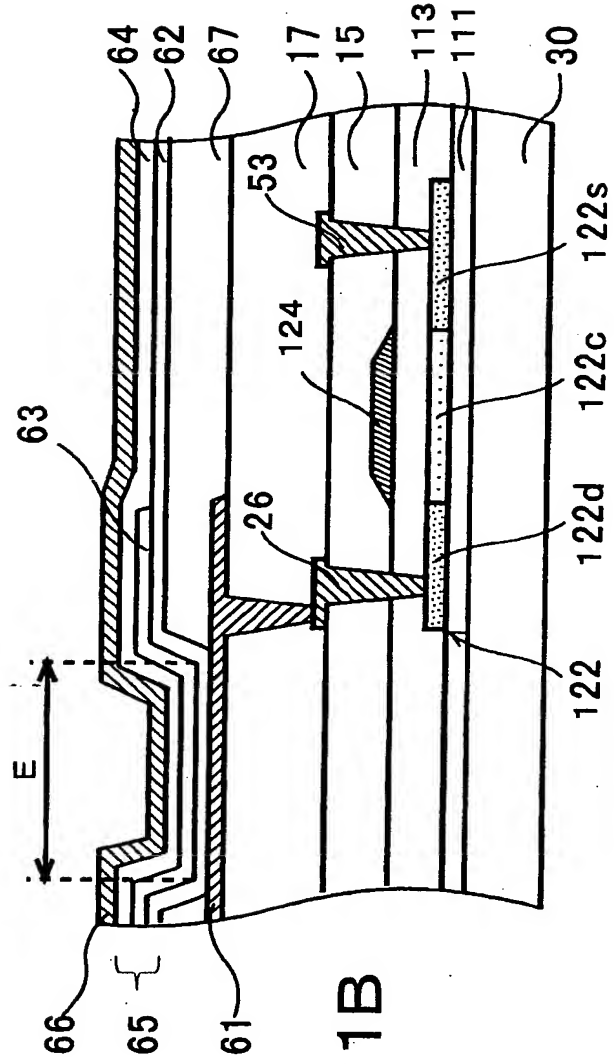


Fig. 11B

This cross-sectional view shows the internal structure of the device. A substrate 30 is composed of layers 111, 113, 15, and 17. A gate stack 61 is formed on the surface, consisting of layers 62, 64, and 66. A gate electrode 26 is positioned within the gate stack. A channel region 124 is located beneath the gate electrode. Source and drain regions 122 and 122d are formed in the substrate. A contact layer 53 is located between the source/drain regions and the substrate. The device is shown in cross-section along line A-A, with a width E indicated.

A detailed cross-sectional diagram of a semiconductor device. The base is a substrate 30 consisting of multiple layers: 111 at the bottom, followed by 113, 15, and 17. In the center, there is a region 124. To its left and right are regions 122d, 122c, and 122s. Above these, there are several more complex structures. On the left, a layer 61 is shown. Above it, a series of layers are grouped as 62, 64, and 63, collectively forming part of a larger structure 65. A layer 66 is also indicated. A dimension E is shown at the top, indicating a width. A dimension B is shown on the left side, indicating a height or thickness. Other labels include 26 and 53 pointing to specific structural features.

Fig. 13A

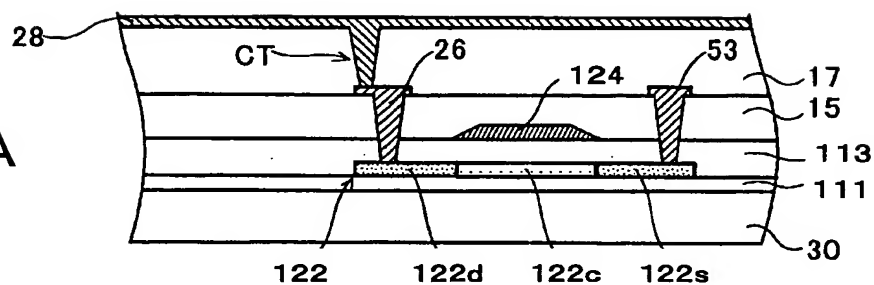


Fig. 13B

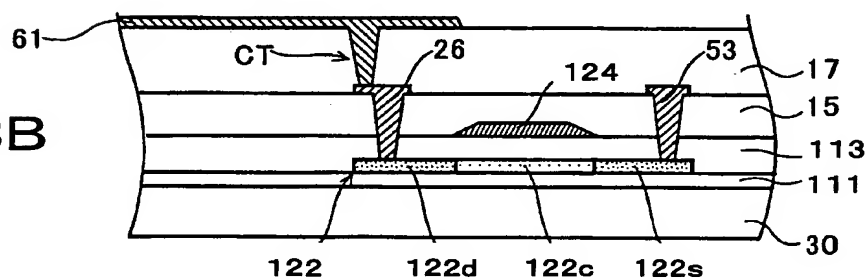


Fig. 13C

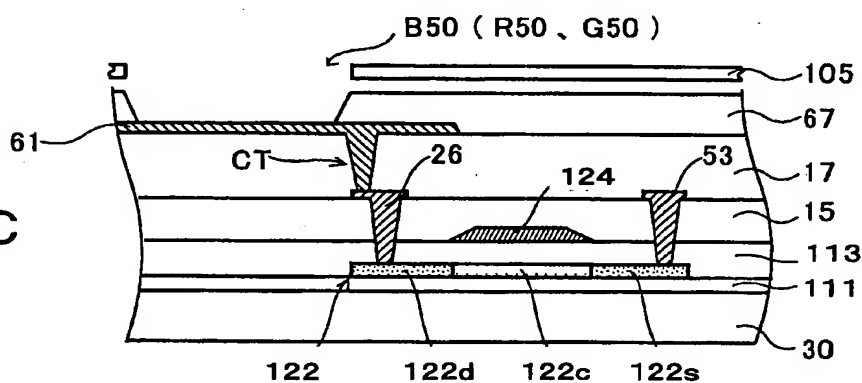
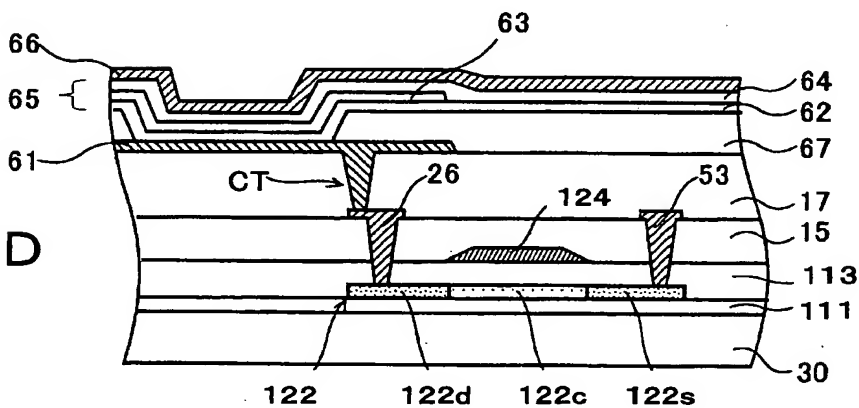


Fig. 13D



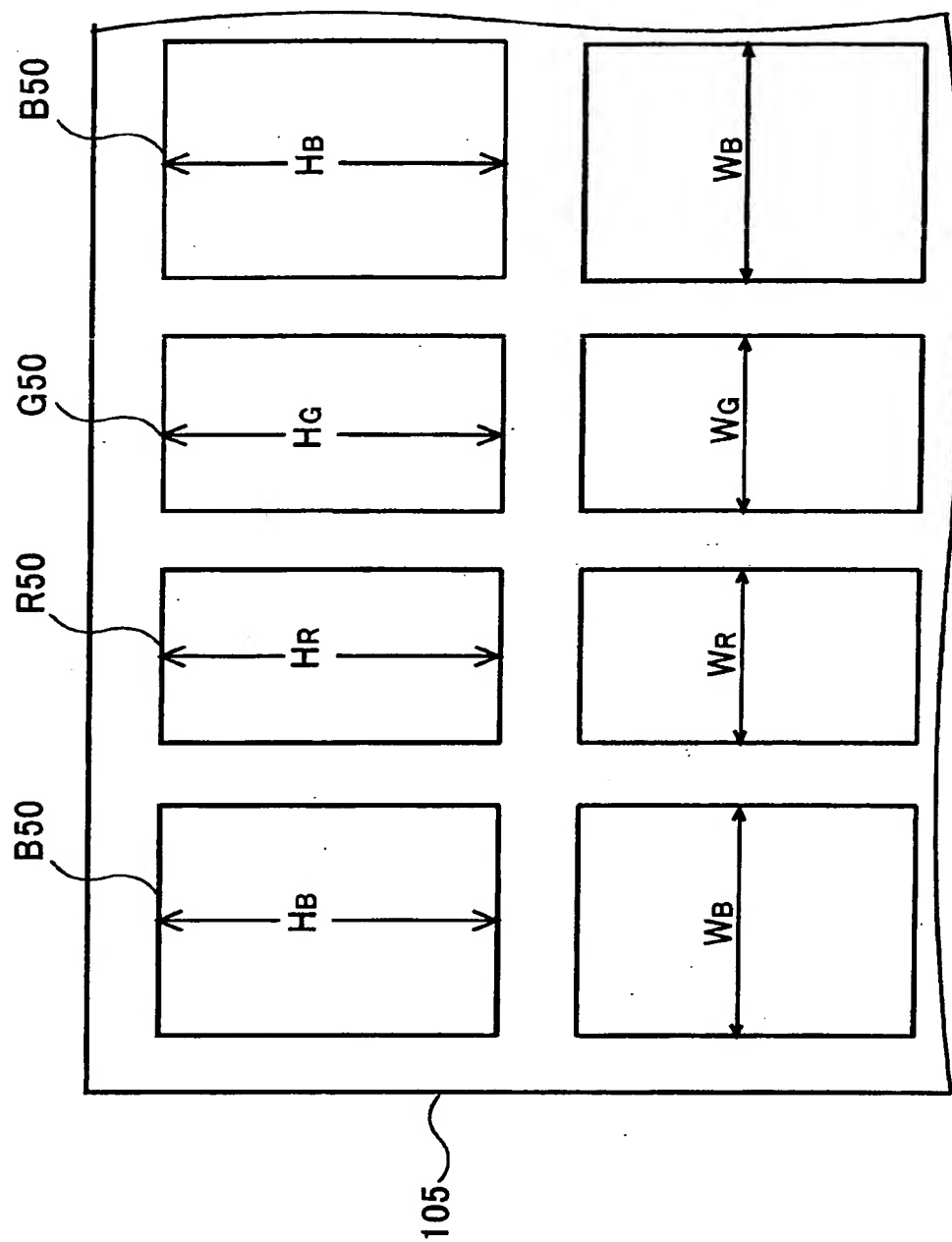


Fig. 14

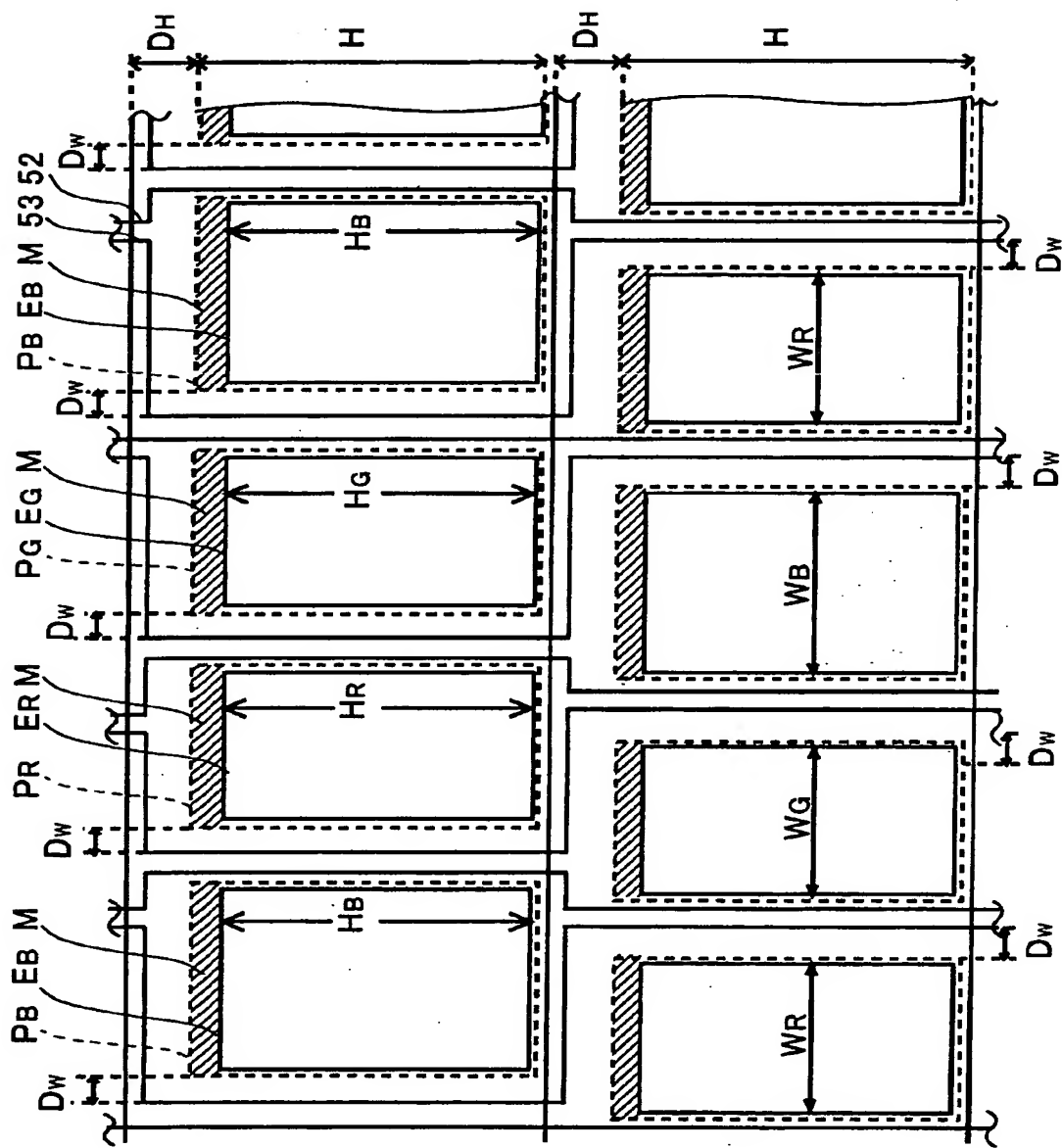


Fig. 15

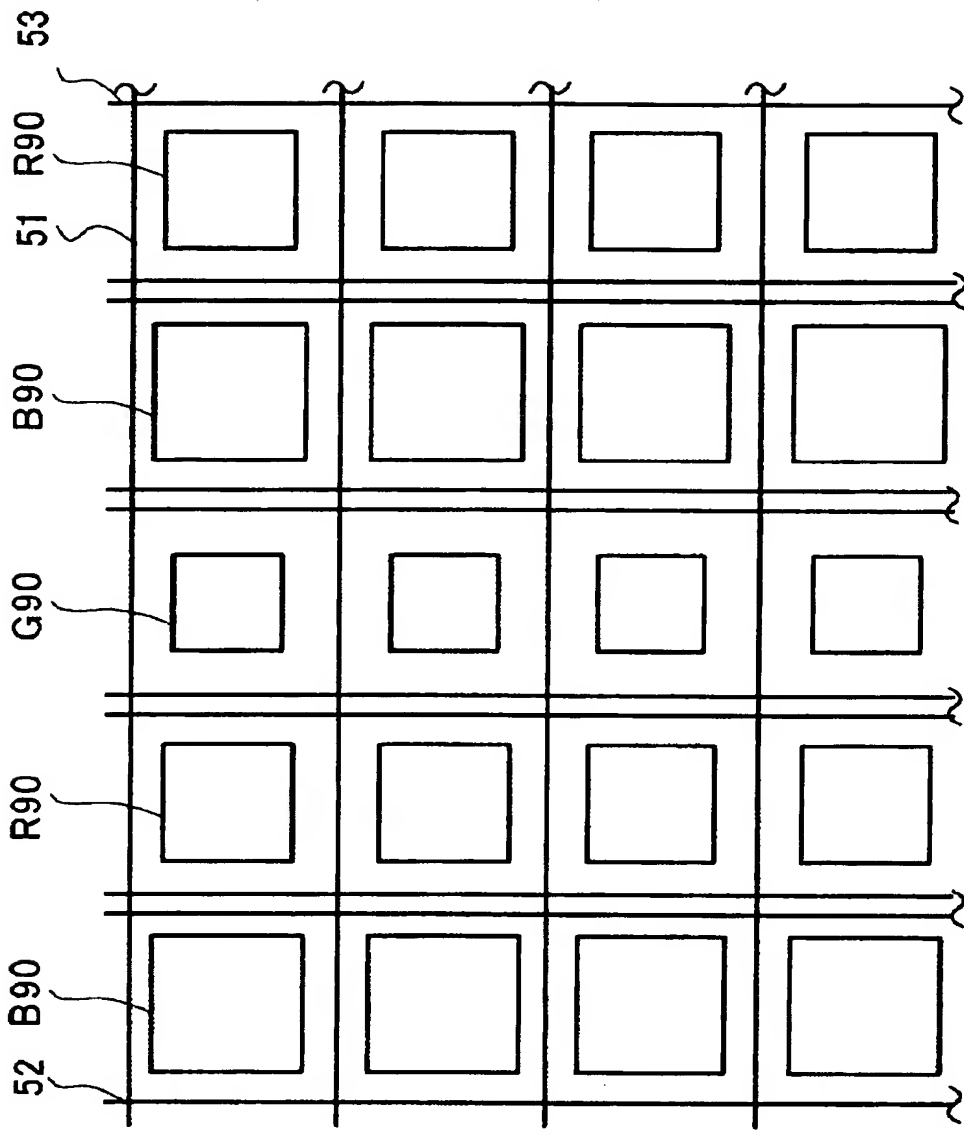


Fig. 16